In the Claims:

1. (Currently Amended) A processor readable medium [storing]encoding a data structure for supporting one or more packet modification operations, the data structure comprising:

a pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area; and

a pointer to a burst of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first.

2. (Original) The processor readable medium of claim 1 wherein the first and second memory areas are located in different memories.

3. (Original) The processor readable medium of claim 1 wherein the first and second memory areas are located in the same memory.

4. (Original) The processor readable medium of claim 1 wherein the one or more commands are stored in a packed format.

5. (Original) The processor readable medium of claim 1 wherein the one or more data or mask items are stored in a packed format.

6. (Original) The processor readable medium of claim 1 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

7. (Original) The processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip from a modification processor configured to execute the one or more commands.

8. (Original) The processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip with the modification processor.

9. (Original) The processor readable medium of claim 1 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.

10. (Original) The processor readable medium of claim 9 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.

11. (Currently Amended) A method of performing one or more packet modification operations on a packet while located within a first portion of a switch, the packet including a data structure index previously added while the packet was located within a second portion of the switch, the method comprising:

retrieving from a memory a data structure corresponding to the data structure index, and comprising a pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in a first memory area, and a pointer to a burst of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first;

retrieving from the first memory area the one or more commands;

retrieving from the second memory area the one or more data or mask items for use by the one or more commands; and

executing the one or more commands by the processor, thereby performing one or more packet modification operations on the packet.

12. (Original) The method of claim 11 wherein the first portion of the switch is an egress portion of the switch.

13. (Original) The method of claim 11 wherein the second portion of the switch is an ingress portion of the switch.

14. (Original) The method of claim 12 wherein the first and second memory areas are located in different memories.

15. (Original) The method of claim 12 wherein the first and second memory areas are located in the same memory.

16. (Original) The method of claim 12 wherein the one or more commands are stored in a packed format.

17. (Original) The method of claim 12 wherein the one or more data or mask items are stored in a packed format.

18. (Original) The method of claim 12 wherein the one or more data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

19. (Original) The method of claim 12 wherein the first and second memory areas are located in a memory implemented off chip from a modification processor which executes the one or more commands.

20. (Original) The method of claim 12 wherein the first memory area is located in a memory implemented on chip with the modification processor.

21. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a sequence of one or more commands implementing one or more packet modification operations.

22. (Original) The method of claim 12 wherein the data structure comprises one or more pointers, each to a burst of one or more data or mask items.

23. (Currently Amended) A method of performing one or more packet modification operations on a packet while located within a first portion of a switch, the packet including a data structure index previously added while the packet was located in a second portion of the switch, the method comprising:

a step for retrieving from a memory a data structure corresponding to the data structure index, and comprising a pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and stored in first memory area, and a pointer to a burst

of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first;

a step for retrieving from the first memory area the one or more commands;

a step for retrieving from the second memory area the one or more data or mask items for use by the one or more commands; and

a step for executing the one or more commands by the processor, thereby performing one or more packet modification operations on the packet.